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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/431,477	11/01/1999	KIRAN GANESH	884.141US1	8764

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EXAMINER
KIK, PHALLAKA

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 06/26/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/431,477	Applicant(s) GANESH ET AL.	
	Examiner Phallaka Kik	Art Unit 2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 April 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4-8,10-23,25-27 and 29-31* is/are pending in the application, wherein claims 3,9,24,27 are cancelled.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-8,10-23,25-27 and 29-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 November 1999* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Response to Amendment

1. This Office Action responds to Applicant's amendment filed 4/4/2002. Claims 1-2,4-8,10-23,25-27,29-31 are pending, wherein claims 1-2,7-8,22,26,29,31 have been amended and claims 3,9,24,28 have been cancelled. Claims 1-2,4-8,10-23,25-27,29-31 have been examined; however, Applicant's arguments are not persuasive; therefore, the previous Office action is incorporated herein.

Drawings

2. The drawings filed on 11/1/1999 are acceptable under the new rules as being easily readable and scannable, as indicated in the previous Office Action.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. **Claims 1-2,4,6-8,10-17,22-23,25-27,29-31** are rejected under 35 U.S.C. 102(b) as being anticipated by **Ito** (US Patent No. 5,648,910).

Ito (US Patent No. 5,648,910) discloses a method of automatically optimizing power supply network executed by a CAD systems and estimates current consumptions of component function blocks, taking into consideration electromigration problems (abstract; col. 4, lines 9-43; Fig. 2).

As per **claims 1-2,4,6-8,11-17,22-23,25-27,29-31**, all of the elements of the claims are illustrated in Fig. 2 (see also col. 4-7), wherein the iterative loops steps/means S7-S11 provides for the rearranging and analyzing steps/means, the layout rule defining a maximum current for a given width is part of step/mean S9, the reliability verification being electromigration is described in abstract; wherein the layout being a two-dimensional layout comprising a plurality of overlapping rows are further illustrated in Figs. 3-8, and wherein the reliability consideration due to self-heating is inherently associated with the electromigration as is well known in the art (see prior arts cited below); wherein the overlapping rows are inherently included as part of the routing/placement problems that often occurs as is well known in the art; wherein the reliability verification factor is the constraint relating to electromigration/self-heating phenomena (i.e., the width of the power supply lines or the wiring interconnects as being based on the current flowing through the wire such that it is free from electromigration/self-heating problems); and since the method is implemented by a CAD system (abstract), the memory, instruction, computer readable medium, and processor are inherently included.

As per **claim 10**, other layout considerations (i.e., layout/routing density) are also described in col. 4, lines 27-43.

5. **Claims 1-2,4,6-8,10-17,22-23,25-27,29-31** are rejected under 35 U.S.C. 102(b) as being anticipated by **Hathaway et al.** (US Patent No. 5,737,580).

Hathaway et al. (US Patent No. 5,737,580) disclose a method of wiring IC chips such that electromigration criteria are met while minimizing the effect on overall chip wireability, including optimizing wire width to adequately support the electromigration current on that net as a function of the capacitive loading of the net itself (abstract; Fig. 2; col. 3, line 1 to col. 5, line 67).

6. As per **claims 1-2,4,6-8,11-17,22-23,25-27,29-31**, all of the elements of the claims are illustrated in Figs. 2-4,6A,6B (see also col. 3, line 1 to col. 5, line 67), wherein the rearranging and analyzing steps/means is further described in col. 5, line 60 to col. 6, line 5, wherein the reliability consideration due to self-heating is inherently associated with the electromigration check as described in col. 5, lines 25-59 wherein such self-heating is always associated with electromigration as is well known in the art (see prior arts cited below), and wherein the overlapping rows are inherently included as part of the routing/placement problems that often occurs as is well known in the art; wherein the reliability verification factor is the constraint relating to electromigration/self-heating phenomena (i.e., the width of the power supply lines or the wiring interconnects as being based on the current flowing through the wire such that it is free from electromigration/self-heating problems); and since the method is implemented by a CAD system (i.e., EDA tools--col. 1, lines 5-12), the memory, instruction, computer readable medium, and processor are inherently included.

As per **claim 10**, other layout considerations (i.e., routing complexity--detailed and global routing; timings) are also described in col. 4, line 31 to col. 5, 25.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.

Patentability shall not be negatived by the manner in which the invention was made.

8. **Claim 5** is rejected under 35 U.S.C. 103(a) as being unpatentable over **Ito** (US Patent No. 5,648,910).

As per **claim 5**, **Ito** discloses all of the elements of the claim as discussed in the rejection of claim 1 above, but failed to particularly teach that the circuit design be a microprocessor design. However, it would have been obvious to one of ordinary skilled in the art at the time of the invention that the circuit design method/apparatus of Ito is also applicable to microprocessor design since microprocessor design are also subjected to electromigration/self-heating problems due to similar technologies as is well known in the art in which the method/apparatus of Ito can be applied.

9. **Claim 5** is rejected under 35 U.S.C. 103(a) as being unpatentable over **Hathaway et al.** (US Patent No. 5,737,580).

As per **claim 5**, **Hathaway et al.** disclose all of the elements of the claim as discussed in the rejection of claim 1 above, but failed to particularly teach that the circuit design be a microprocessor design. However, it would have been obvious to one of ordinary skilled in the art at the time of the invention that the circuit design method/apparatus of **Hathaway et al.** is also applicable to microprocessor design since microprocessor design are also subjected to electromigration/self-heating problems due to similar technologies as is well known in the art in which the method/apparatus of **Hathaway et al.** can be applied.

10. **Claims 18-21** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Hathaway et al.** (US Patent No. 5,737,580) in view of **Gupta et al.** ("Optimal 2-D cell

layout with integrated transistor folding", 1998 IEEE/ACM International Conference on Computer-Aided Design, 8 November 1998, pp. 128-135).

Gupta et al. disclose a technique that integrates folding into the generation of optimal layouts of CMOS cells in the two dimensional style to optimize some cost function under a set of constraints such as cell area and/or delay optimization (abstract; sections 3-6).

As per **claims 18-21**, **Hathaway et al.** disclose all of the elements of the claims as discussed in the rejection of claim 14 which the claims depend. However, **Hathaway et al.** failed to further teach the adjusting of one or more of the components in one of the clusters to comply with a size constraint (i.e., device-based legging, stack-based legging, differential legging). Such methods for further compacting the transistors is well known in the art as further taught by **Gupta et al.** to further optimize the cells of the pluralities of integrated circuit components under a set of constraints (abstract; sections 2-6). It would have been obvious to one of ordinary skilled in the art at the time of the invention to further incorporate the compacting/transistor folding method of **Gupta et al.** into the system/method of **Hathaway et al.** because such compacting/transistor folding method would further optimizes the integrated circuit components cell layouts as is well known in the art.

Remarks

11. As per **claims 1-4,6-31**, Applicant argued that neither **Ito** nor **Hathaway et al.** discloses the layout rules based on a reliability verification constraints arising from self heat, as amended, wherein **Ito** describes regulating width of each power supply line incorporated in the power supply network on the basis of current passing therethrough so that the power supply network is free from electromigration, and wherein **Hathaway et al.** describes a technique to optimize the width of automatically routed wire segments

so that these widths are adequate to support the electromigration current on the net as a function of the capacitive loading of the net itself. Applicant further argued that neither **Ito** nor **Hathaway et al.** describe minimizing a cost function having reliability verification factor. The Examiner is not persuaded. First of all, the Examiner agrees that the term "self-heating" is not cited in either **Ito** or **Hathaway et al.** as pointed out by Applicant. However, as stated by the Examiner in the previous Office action, the "self-heating" are associated with electromigration problems; that is, by controlling the current flowing through the wires or routings interconnects, both the electromigration and self-heating phenomena are solved. Thus self-heating and electromigration are two phenomena which are inherently related to each other by the amount of current flowing through the wiring interconnects, as taught in the recited prior arts made of record (see **Gardner**, US Patent No. 5,817,574, especially col. 1, lines 52-57; col. 4, lines 16-67; **Teng et al.**, ("iTEM: a temperature-dependent electromigration reliability diagnosis tool", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 16, No. 8, August 1997, pp. 882-893, especially abstract and section V; and **Myscore et al.**, US Patent No. 6,308,303, especially col. 1, lines 40-52; col. 6, line 62 to col. 7, line 13). Accordingly, since both the methods of **Ito** and **Hathaway et al.** (especially col. 3, lines 1-14) solve this problem by controlling the current flowing through the wires/routing interconnects by using the appropriate wire widths that avoids the electromigration phenomenon, self-heating phenomenon is inherently considered. Applicant should especially note that **Myscore et al.** clearly teach this phenomena as part of the background art that "electromigration and self-heating phenomena place constraints on the minimum allowed width of a wire, depending on the current flow through the wire" (col. 1, lines 40-52) and further shows this minimum wire width as a function of self heat coefficient and rms current (col. 7, lines 7-13). Secondly, the reliability verification factor

is the constraint relating to electromigration/self-heating phenomena (i.e., the width of the power supply lines or the wiring interconnects as being based on the current flowing through the wire such that it is free from electromigration/self-heating problems).

12. As per **claim 5**, in response to Applicant's request for a reference to support the Examiner's position that the reliability verification (i.e., due to electromigration and/or self-heating) for the circuit design also apply to microprocessor design, the attached prior arts are given (see **Dalal et al.** as previously cited; **Malinoski et al.** and **Aipperspach et al.** below).

Conclusion

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Therefore, Applicants are requested to carefully consider them in response to this Office Action. In particular, the following prior arts made of record are most relevant:

Gardner (US Patent No. 5,817,574) discloses a method of forming a high surface area interconnection structure, taking into consideration reliability factor such as electromigration and self-heating problems (abstract; col. 1, lines 42-57; col. 4, lines 16-67).

Teng et al. ("iTEM: a temperature-dependent electromigration reliability diagnosis tool", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 16, No. 8, August 1997, pp. 882-893) disclose an electromigration reliability diagnosis tool for CMOS VLSI circuits which can estimate the interconnect temperature rise due to joule heating and heat conduction from the substrate using lumped thermal model (abstract; section V).

Dalal et al. ("Design of an efficient power distribution network for the UltraSPARC0I microprocessor", Proceedings of 1995 IEEE International Conference on

Computer Design: VLSI in Computers and Processors, 2 October 1995, pp. 118-123) disclose the design, implementation and verification of the power distribution network for the 5.2 million transistor UltraSPARC-I microprocessor wherein a simulation method allows rapid identification of exact layout locations with potential electromigration or excessive voltage drop problems (abstract; sections 3-5).

Malinoski et al. (« A test site thermal control system for at-speed manufacturing testing », Proceedings of the 1998 International Test Conference, 18 October 1998, pp. 119-128, especially abstract).

Aipperspach et al. (« A 0.2-/spl mu/m, 1.8V, SOI, 550-MHZ, 64-b PowerPC Micropocessor with Copper Interconnects", IEEE Journal of Solid-State Circuits, Vol. 34, No. 11, 15 February 1999, pp. 1430-1435, especially abstract and section III, D).

14. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phallaka Kik whose telephone number is 703-306-3039. The examiner can normally be reached on Flexitime.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on 703-308-1323. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-1782.

Any response to this action should be mailed to:

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Hand-delivered responses should be brought to Crystal Plaza 4, 2201 South Clark Place, Arlington, VA 22202, Fourth Floor (Receptionist).

PK
June 19, 2002

VUTHE SIEK
Primary Examiner